MP0393 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appeal No. _____

Application No.:	10/666,892
Filing Date:	September 17, 2003
Appellants:	Hong-Yi Hubert Chen et al.
Conf. No.:	
Group Art Unit:	2186
Examiner:	Hetul B. Patel
Title:	MEMORY MAPPED REGISTER FILE AND METHOD FOR ACCESSING THE SAME

BRIEF ON APPEAL ON BEHALF OF APPELLANTS

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February 13, 2009

Sir:

This brief on appeal is submitted pursuant to the Notice of Appeal filed in the U.S. Patent and Trademark Office on December 17, 2008, and from the decision of the Patent Examiner dated August 15, 2008, rejecting claims 1-10, 13-23, 25, 26, and 51-79 as set forth in the Final Action mailed March 21, 2008.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The present application is assigned to Marvell International Ltd. by virtue of assignments recorded in the Patent and Trademark Office at Reel 014535, Frame 0015 and Reel 014535, Frame 0032.

II. RELATED APPEALS AND INTERFERENCES

The undersigned, the Assignee, and the Appellants do not know of any other appeals or interferences which would directly affect or that would be directly affected by, or have a bearing on, the Board's decision in this Appeal.

III. STATUS OF THE CLAIMS

Claims 1-10, 12-23, 25, 26 and 51-79 are currently pending, and are reproduced in the attached Claims Appendix. Claims 11, 24, 27-50 and 80-85 are cancelled. Appellants traverse and appeal the rejection of claims 1-10, 12-23, 25, 26 and 51-79.

IV. STATUS OF THE AMENDMENTS

The claims have not been amended subsequent to the final rejection, and there are no unentered amendments.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Independent claim 1 recites a register system (e.g., register file 206, FIG. 2; see Page 9, Lines 3-4) for a data processing system (e.g., data processing system 200, FIG. 2; see Page 9, Lines 3-4) that includes an unbanked memory unit (e.g., register file memory unit 400, FIG. 4; see Page 12, Lines 13-21) having a plurality of memory locations (e.g., registers, FIG. 4; see Page 13, Lines 1-2), each memory location being addressable by an encoded address (e.g., FIG. 4; see Page 13, Lines 2-4), wherein the encoded address corresponds to at least one register and processor mode (e.g., FIG. 4; see Page 13, Lines 5-7). Input ports (e.g., inputs, FIG. 3; see Page 11, Lines 8-10) receive inputs for addressing at least one of the memory locations using an encoded address (e.g., FIG. 3; see Page 12, Lines 7-11). Output ports (e.g., source data outputs, FIG. 3; see Page 11, Lines 11-12) output data from at least one of the memory locations addressable by an encoded address (e.g., FIG. 3; see Page 12, Lines 1-4). The register system includes a plurality of address encoders (e.g., address encoders 402 and 410, FIG. 4; see Page 12, Lines 15-17), a respective one of the plurality of address encoders for each of the input ports (e.g., as shown in FIG. 4). Each of the address encoders provides an encoded address for accessing one of the memory locations (e.g., FIG. 4; see Page 13, Lines 17-22).

Independent claim 14 recites a register system (e.g., register file 206, FIG. 2; see Page 9, Lines 3-4) for a data processing system (e.g., data processing system 200, FIG. 2; see Page 9, Lines 3-4) that includes unbanked memory means (e.g., register file memory unit 400, FIG. 4; see Page 12, Lines 13-21) having a plurality of memory locations (e.g., registers, FIG. 4; see Page 13, Lines 1-2), each memory location being addressable by an encoded address (e.g., FIG. 4; see Page 13, Lines 2-4), wherein the encoded address corresponds to at least one register means and processor mode (e.g., FIG. 4; see Page 13, Lines 5-7), a plurality of input means (e.g., inputs, FIG. 3; see Page 11, Lines 8-10) to receive inputs for addressing at least one of the memory locations using an encoded address (e.g., FIG. 3; see Page 12, Lines 7-11), output means (e.g., source data outputs, FIG. 3; see Page 11, Lines 11-12) to

output data from at least one of the memory locations addressable by an encoded address (e.g., FIG. 3; see Page 12, Lines 1-4), and a plurality of addressing means (e.g., address encoders 402 and 410, FIG. 4; see Page 12, Lines 15-17), one of the addressing means for each of the input means (e.g., as shown in FIG. 4), each of the addressing means to provide an encoded address for accessing one of the memory locations (e.g., FIG. 4; see Page 13, Lines 17-22).

Independent claim 51 recites a processor (e.g., data processing system 200, FIG. 2; see Page 9, Lines 3-4) that includes an integrated circuit (e.g., data processing system 200, FIG. 2; see Page 9, Lines 9-10). The integrated circuit includes an unbanked memory unit (e.g., register file memory unit 400, FIG. 4; see Page 12, Lines 13-21) having a plurality of memory locations (e.g., registers, FIG. 4; see Page 13, Lines 1-2), each memory location being addressable by an encoded address (e.g., FIG. 4; see Page 13, Lines 2-4), wherein the encoded address corresponds to at least one register and processor mode (e.g., FIG. 4; see Page 13, Lines 5-7). The integrated circuit includes a plurality of address encoders (e.g., address encoders 402 and 410, FIG. 4; see Page 12, Lines 15-17) to provide at least one encoded address for addressing at least one of the memory locations (e.g., FIG. 4; see Page 13, Lines 17-22).

Independent claim 61 recites a data processing system (e.g., data processing system 200, FIG. 2; see Page 9, Lines 3-4) that includes a memory mapped register system (e.g., register file 206, FIG. 2; see Page 9, Lines 3-4) for accessing a plurality of memory locations (e.g., registers, FIG. 4; see Page 13, Lines 1-2), each memory location being addressable by an encoded address (e.g., FIG. 4; see Page 13, Lines 2-4), wherein the encoded address corresponds to at least one register and processor mode (e.g., FIG. 4; see Page 13, Lines 5-7), and a plurality of address encoders (e.g., address encoders 402 and 410, FIG. 4; see Page 12, Lines 15-17), a respective one of the plurality of address encoders for each of a plurality of input ports of the register system (e.g., as shown in FIG. 4). Each of the address encoders provides an encoded address for accessing one of the memory locations (e.g., FIG. 4; see Page 13, Lines 17-22).

Independent claim 64 recites a processor (e.g., data processing system 200, FIG. 2; see Page 9, Lines 3-4) that includes circuit means (e.g., data processing system 200, FIG. 2; see Page 9, Lines 9-10). The circuit means includes unbanked memory means (e.g., register file memory unit 400, FIG. 4; see Page 12, Lines 13-21) having a plurality of memory locations (e.g., registers, FIG. 4; see Page 13, Lines 1-2), each memory location being addressable by an encoded address (e.g., FIG. 4; see Page 13, Lines 2-4), wherein the encoded address corresponds to at least one register means and processor mode (e.g., FIG. 4; see Page 13, Lines 5-7), and a plurality of addressing means (e.g., address encoders 402 and 410, FIG. 4; see Page 12, Lines 15-17) to provide at least one encoded address for addressing at least one of the memory locations (e.g., FIG. 4; see Page 13, Lines 17-22).

Independent claim 74 recites an integrated circuit method that includes configuring the integrated circuit (e.g., data processing system 200, FIG. 2; see Page 9, Lines 9-10) to receive a plurality of inputs (e.g., inputs, FIG. 3; see Page 11, Lines 8-10), configuring the integrated circuit to determine an unbanked encoded address (e.g., FIG. 4; see Page 13, Lines 2-4) based on the received inputs, wherein the unbanked encoded address corresponds to at least one register and processor mode (e.g., FIG. 4; see Page 13, Lines 5-7), receiving the plurality of inputs from a plurality of address encoders (e.g., address encoders 402 and 410, FIG. 4; see Page 12, Lines 15-17), configuring the integrated circuit to access a register using an unbanked encoded address (e.g., FIG. 4; see Page 13, Lines 1-2), and configuring the integrated circuit to output data from the accessed register (e.g., via outputs, FIG. 3; see Page 12, Lines 1-4).

Independent claim 78 recites a method for accessing an unbanked memory unit (e.g., register file memory unit 400, FIG. 4; see Page 12, Lines 13-21) having a plurality of memory locations (e.g., registers, FIG. 4; see Page 13, Lines 1-2). The method includes receiving a memory request for accessing the unbanked memory unit at one of a plurality of address encoders (e.g., address encoders 402 and 410, FIG. 4; see Page 12, Lines 15-17), the memory request including a register index input and a processor mode input (e.g., FIG. 4; see Page 13, Lines 5-7), encoding the register index input and processor mode input at the one of the plurality of address encoders

(e.g., FIG. 4; see Page 13, Lines 15-20) to obtain an encoded address (e.g., FIG. 4; see Page 13, Lines 1-2), accessing at least one of the memory locations of the unbanked memory unit in accordance with the encoded address (e.g., FIG. 4; see Page 13, Lines 17-22), wherein the encoded address corresponds to at least one register and processor mode (e.g., FIG. 4; see Page 13, Lines 2-6), and writing data into or reading data from the accessed memory location (e.g., via wr and source data lines, respectively, as shown in FIG. 4; see Page 13, Lines 22-23 and Page 14, Lines 17-18).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Appellants seek the Board's review of the rejection of:

(a) claims 1-10, 14-23, 51-56, 60-69 and 73-79 under 35. U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,701,493 ("Jaggar") in view of U.S. Patent No. 5,809,528 ("Miller").

(b) claims 1-10, 14-23, 51-79 under 35. U.S.C. 103(a) as being unpatentable over Jaggar.

(c) claims 12-13 and 25-26 under 35. U.S.C. 103(a) as being unpatentable over Jaggar and Miller, and further in view of U.S. Patent No. 6,363,471 ("Meier").

(c) claims 12-13 and 25-26 under 35. U.S.C. 103(a) as being unpatentable over Jaggar in view of Meier.

VII. ARGUMENTS

A. The Rejections

The Examiner rejected each of independent claims 1, 14, 51, 61, 64, 74 and 78 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Jaggar in view of Miller; and rejected each of independent claims 1, 14, 51, 61, 64, 74, and 79 under 35. U.S.C. 103(a) as being unpatentable over Jaggar

In both rejections, the Examiner acknowledges that Jaggar does not disclose a plurality of encoders, in which each encoder is for a corresponding input port. (See Page 3, Lines 19-20 and Page 8, Lines 10-12 of the Office Action mailed August 15, 2008, hereinafter "the Office Action"). The Examiner, however, relies on Miller to disclose "having N address encoders one for each input," citing Column 6, Lines 23-35 and FIG. 2A, element 102. (See Page 3, Lines 20-22 of the Office Action). Alternatively, the Examiner alleges that duplicating a common address encoder as taught by Jaggar would be obvious. (See Page 8, Lines 12-15 of the Office Action).

B. Claim Distinctions

1. Distinctions regarding independent Claims 1, 14, 51, 61, 64, 74 and 78

Claim 1 recites a register system for a data processing system. The register system includes input ports (to receive inputs for addressing a memory location) and a plurality of address encoders. Each address encoder is for a corresponding input port, and each address encoder provides an encoded address for accessing a memory location.

For example, as shown in an exemplary embodiment in FIG. 4 of the present application, a register file 206 includes a register file memory unit 400 and a plurality of address encoders including, for example, address encoders 402_1, 402_2, 4023, 402_4, 410_1, and 410_2. Each of the address encoders receives a plurality of inputs. For example, the address encoder 402_1 receives a processor mode input and a srcl.index input. In other words, each of the inputs to the register file memory unit 400 includes a corresponding address encoder.

(a) *Jaggar Fails To Disclose an Address Encoder for a Corresponding Input Port as recited in Claim 1*

In rejecting claim 1, the Examiner alleges that Jaggar discloses "an address encoder to provide an encoded address," relying on "the combination of components 12-20 in Fig. 8" (see pg. 3 of Final Rejection). Appellants respectfully note that FIG. 8

of Jaggar does not disclose a plurality of address encoders as claim 1 recites. Instead, FIG. 8 of Jaggar discloses only a single address encoder (i.e., the components 12-20 make up the single address encoder) for all of the registers.

Further, in rejecting claim 1, the Examiner alternatively alleges that providing a plurality of address encoders as claim 1 recites would be obvious to one skilled in the art "simply by duplicating the common address encoder taught by...Jaggar at both input ports." Appellants respectfully disagree and submit that Jaggar teaches away from such a duplication. For example, the alleged encoder of Jaggar receives all register addresses and processor modes at the same encoder and communicates over a single common bus 4. Accordingly, there would be no advantage whatsoever in merely "duplicating" the alleged encoder of Jaggar. Instead, the encoder, as well as the communication bus, would necessarily have to be modified in order to justify simple duplication. In other words, there are inherent structural differences in the common encoder of Jaggar.

For example, the Examiner further alleges that modifying Jaggar to simply duplicate the common encoder "increases the overall performance of the data processing system by providing the encoded addresses for all inputs in parallel compared to one by one." Appellants respectfully disagree and submit that duplicating the encoder, without also modifying the encoder and the bus structure of Jaggar, would not improve performance. Instead of one common encoder that converts all addresses and processor modes to encoded addresses, multiple encoders would be converting all address and processor modes to encoded addresses and communicating the encoded addresses over the same common bus. The resulting unnecessary redundancy and increased bus traffic would not increase the performance of Jaggar. Accordingly, Appellants respectfully submit that if a person skilled in the art was motivated to improve the performance Jaggar, that person would not duplicate the common address encoder due to Jaggar's bus structure.

In response, the Examiner alleges that simply duplicating components 12-20 of Jaggar, which purportedly correspond to a single decoder, "both input ports will have different encoded addresses inputted to access different registers." (See Page 2 of the Advisory Action). Appellants respectfully disagree and note that the alleged

components 12-20 include a single register address decoder 17 that receives a composite register address, compares the composite register address with all stored addresses, and addresses one of the registers based on the comparison. (See Column 3, Lines 18-33). In other words the decoder 17 appears to communicate with every alleged register. Duplicating the decoder 17 as the Examiner suggests would result in multiple decoders 17 and every one of the decoders 17 would receive the composite address, compare the composite address with all stored addresses, and potentially communicate with every register as shown in FIG. 8 of Jaggar. Accordingly, Appellants respectfully maintain that merely duplicating components 12-20 of Jaggar would not be obvious.

(b) *Miller Fails To Disclose an Address Encoder for a Corresponding Input Port as recited in Claim 1*

Appellants respectfully submit that Miller fails to make up for the deficiencies of Jaggar. For example, the Examiner cites Column 6, Lines 23-35 and element 102 in FIG. 2A in support of the allegation that Miller discloses "having N address encoders one for each input." Appellants respectfully disagree and submit that Miller discloses, at best, the same two encoders associated with all of the inputs.

More specifically, Appellants respectfully note that the cited portions of Miller fail to disclose a respective one of the plurality of address encoders for each of the input ports. In other words, Appellants' claim limitation requires that each input port has its own address encoder, which is implicit in the term "respective." In contrast, all of the input ports of Miller appear to share the same encoders.

For example, FIG. 2A of Miller discloses two entry address encoders 102 and 123 and a register stack 110. The register stack 110 includes 32 registers and corresponding input ports. Appellants respectfully note that both of the address encoders 102 and 123 communicate with all 32 registers via the same address buses 218 and 220. Accordingly, this structure is not analogous to a respective one of a plurality of address encoders for each of the input ports.

In response, the Examiner states that Miller discloses a respective one of the plurality of address encoders for each of the input ports. (See Page 2 of the Advisory

Action). Appellants respectfully disagree and again note that, at best, multiple input ports that share the same encoders. Appellants respectfully submit that sharing, for example, two encoders for a significantly larger number of input ports is not analogous to a "respective one of a plurality of address encoders for each of the input ports." More specifically, Appellants respectfully submit the term respective requires that each of the input ports is associated with an individual and independent address encoder. If the address encoders are shared, the term "respective" would not be proper. Further, **each** of the input ports is associated with a respective one of the address encoders. In other words, **all** of the input ports have a corresponding (or dedicated) encoder. Accordingly, Appellants respectfully assert that a plurality of input ports sharing two encoders does not disclose this limitation.

(c) ***The Examiner has failed to establish a prima facie case of obviousness***

To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Both Jaggar and Miller clearly fail to disclose a plurality of address encoders, in which each address encoder is for a corresponding input port. Consequently, the combination of Jaggar and Miller cannot render claim 1 obvious.

In view of the foregoing, Appellants respectfully submit that claim 1, as well as its dependent claims, should be allowable for at least the above reasons. Claims 14, 51, 64, 74, and 78, as well as their corresponding dependent claims, should be allowable for at least similar reasons.

2. Dependent Claims 2-10, 12, 13, 15-23, 25, 26, 52-60, 62, 63, 65-73, and 75-76

With regard to claims 22-10, 12, 13, 15-23, 25, 26, 52-60, 62, 63, 65-73 and 75-76 these claims are allowable for at least the reasons previously presented with regard

to claims 1, 14, 51, 61, 64, 74 and 78, respectively. Accordingly, it is respectfully requested that the rejection of these claims be overturned.

CONCLUSION

Appellants respectfully request the Board to reverse the Examiner's rejection of the claims on appeal. Appellants respectfully submit that Jaggar and Miller does not teach or suggest one or more limitations of the claims as discussed above.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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VIII. CLAIMS APPENDIX

This is a complete and current listing of the claims.

1. (Previously Presented) A register system for a data processing system comprising:

an unbanked memory unit having a plurality of memory locations, each memory location being addressable by an encoded address, wherein the encoded address corresponds to at least one register and processor mode;

input ports to receive inputs for addressing at least one of the memory locations using an encoded address;

output ports to output data from at least one of the memory locations addressable by an encoded address; and

a plurality of address encoders, a respective one of the plurality of address encoders for each of the input ports, each of the address encoders to provide an encoded address for accessing one of the memory locations.

2. (Previously Presented) The register system of claim 1, wherein a plurality of registers correspond to the plurality of memory locations of the unbanked memory unit.

3. (Previously Presented) The register system of claim 2, wherein each register is addressable by a corresponding encoded address.

4. (Previously Presented) The register system of claim 3, wherein at least two registers are capable of being accessed in different processor modes using the same encoded address.

5. (Previously Presented) The register system of claim 1, wherein the plurality of memory locations are discontinuous in the unbanked memory unit.

6. (Previously Presented) The register system of claim 1, wherein a bit width of the plurality of memory locations is scalable to any arbitrary bit width size.

7. (Previously Presented) The register system of claim 2, wherein inputs are received associated with at least one register and processor mode, and wherein at least one of the outputs is data from a register associated with an encoded address obtained from the received inputs.

8. (Previously Presented) The register system of claim 7, wherein data is outputted from the unbanked memory unit for at least two instructions.

9. (Previously Presented) The register system of claim 2, wherein inputs are associated with at least one register and processor mode, and wherein one of the inputs is data to be written in a register associated with an encoded address obtained from the received inputs.

10. (Previously Presented) The register system of claim 9, wherein data for at least two retired instructions is to be written in at least two registers.

11. (Cancelled)

12. (Previously Presented) The register system of claim 1, further comprising:

latches to latch an encoded address from respective ones of the address encoders; and

selectors coupled to respective ones of the latches and the address encoders, the selectors to select the encoded address from either the latches or the address encoders.

13. (Previously Presented) The register system of claim 10, wherein the latches store the encoded address as a pipeline storage of the encoded address.

14. (Previously Presented) A register system for a data processing system comprising:

unbanked memory means having a plurality of memory locations, each memory location being addressable by an encoded address, wherein the encoded address corresponds to at least one register means and processor mode;

a plurality of input means to receive inputs for addressing at least one of the memory locations using an encoded address;

output means to output data from at least one of the memory locations addressable by an encoded address; and

a plurality of addressing means, one of the addressing means for each of the input means, each of the addressing means to provide an encoded address for accessing one of the memory locations.

15. (Previously Presented) The register system of claim 14, wherein a plurality of register means correspond to the plurality of memory locations of the unbanked memory means.

16. (Previously Presented) The register system of claim 15, wherein each register means is addressable by a corresponding encoded address.

17. (Previously Presented) The register system of claim 16, wherein at least two register means are capable of being accessed in different processor modes using the same encoded address.

18. (Previously Presented) The register system of claim 14, wherein the plurality of memory locations are discontinuous in the unbanked memory means.

19. (Previously Presented) The register system of claim 14, wherein a bit width of the plurality of memory locations is scalable to any arbitrary bit width size.

20. (Previously Presented) The register system of claim 16, wherein inputs are received associated with at least one register means and processor mode, and wherein at least one of the outputs is data from a register means associated with an encoded address obtained from the received inputs.

21. (Previously Presented) The register system of claim 20, wherein data is outputted from the unbanked memory means for at least two instructions.

22. (Previously Presented) The register system of claim 15, wherein inputs are associated with at least one register means and processor mode, and wherein one of the inputs is data to be written in a register means associated with an encoded address obtained from the received inputs.

23. (Previously Presented) The register system of claim 22, wherein data for at least two retired instructions is to be written in at least two register means.

24. (Cancelled)

25. (Previously Presented) The register system of claim 14, further comprising:

a plurality of latching means to latch an encoded address from respective ones of the addressing means; and

a plurality of selecting means coupled to respective ones of the latching means and the addressing means, the selecting means to select the encoded address from either the latching means or the addressing means.

26. (Previously Presented) The register system of claim 23, wherein the latching means stores the encoded address as a pipeline storage of the encoded address.

27-50. (Cancelled)

51. (Previously Presented) A processor comprising:

an integrated circuit including:

an unbanked memory unit having a plurality of memory locations, each memory location being addressable by an encoded address, wherein the encoded address corresponds to at least one register and processor mode; and

a plurality of address encoders to provide at least one encoded address for addressing at least one of the memory locations.

52. (Previously Presented) The processor of claim 51, wherein a plurality of registers correspond to the plurality of memory locations in the unbanked memory unit.

53. (Original) The processor of claim 52, wherein each register is addressable by a corresponding encoded address.

54. (Original) The processor of claim 53, wherein at least two registers are capable of being accessed in different processor modes using the same encoded address.

55. (Previously Presented) The processor of claim 51, wherein the plurality of memory locations are discontinuous in the unbanked memory unit.

56. (Original) The processor of claim 51, wherein a bit width of the plurality of memory locations is scalable to any arbitrary bit width size.

57. (Original) The processor of claim 51, wherein each address encoder includes input ports to receive inputs associated with at least one register and processor mode in providing a corresponding encoded address.

58. (Original) The processor of claim 57, wherein each address encoder includes logic circuitry to obtain the corresponding encoded address based on the received inputs.

59. (Original) The processor of claim 58, wherein the logic circuitry includes at least one of a programmable gate array (PGA) or a field programmable gate array (FPGA).

60. (Original) The processor of claim 51, wherein the processor is at least one of an embedded processor and a microprocessor.

61. (Previously Presented) A data processing system comprising:

a memory mapped register system for accessing a plurality of memory locations, each memory location being addressable by an encoded address, wherein the encoded address corresponds to at least one register and processor mode; and

a plurality of address encoders, a respective one of the plurality of address encoders for each of a plurality of input ports of the register system, each of the address encoders to provide an encoded address for accessing one of the memory locations.

62. (Original) The data processing system of claim 61, wherein a plurality of registers correspond to the plurality of memory locations.

63. (Original) The data processing system of claim 62, wherein each register is addressable by a corresponding encoded address.

64. (Previously Presented) A processor comprising:

circuit means including:

unbanked memory means having a plurality of memory locations, each memory location being addressable by an encoded address, wherein the encoded address corresponds to at least one register means and processor mode; and

a plurality of addressing means to provide at least one encoded address for addressing at least one of the memory locations.

65. (Previously Presented) The processor of claim 64, wherein a plurality of register means correspond to the plurality of memory locations of the unbanked memory means.

66. (Original) The processor of claim 65, wherein each register means is addressable by a corresponding encoded address.

67. (Original) The processor of claim 66, wherein at least two register means are capable of being accessed in different processor modes using the same encoded address.

68. (Previously Presented) The processor of claim 64, wherein the plurality of memory locations are discontinuous in the unbanked memory means.

69. (Original) The processor of claim 64, wherein a bit width of the plurality of memory locations is scalable to any arbitrary bit width size.

70. (Original) The processor of claim 64, wherein each addressing means includes input means to receive inputs associated with at least one register means and processor mode in providing a corresponding encoded address.

71. (Original) The processor of claim 70, wherein each addressing means includes logic means to obtain the corresponding encoded address based on the received inputs.

72. (Original) The processor of claim 71, wherein the logic means includes at least one of a programmable gate array (PGA) or a field programmable gate array (FPGA).

73. (Original) The processor of claim 64, wherein the processor is at least one of an embedded processor and a microprocessor.

74. (Previously Presented) An integrated circuit method comprising:

configuring the integrated circuit to receive a plurality of inputs;

configuring the integrated circuit to determine an unbanked encoded address based on the received inputs, wherein the unbanked encoded address corresponds to at least one register and processor mode;

receiving the plurality of inputs from a plurality of address encoders;

configuring the integrated circuit to access a register using an unbanked encoded address; and

configuring the integrated circuit to output data from the accessed register.

75. (Original) The method of claim 74, further comprising:

configuring the integrated circuit to output data for multiple instructions.

76. (Original) The method of claim 74, further comprising:

configuring the integrated circuit to write data to the accessed register.

77. (Original) The method of claim 76, further comprising:

configuring the integrated circuit to write data to one or more accessed registers for multiple executed instructions.

78. (Previously Presented) A method for accessing an unbanked memory unit having a plurality of memory locations comprising:

receiving a memory request for accessing the unbanked memory unit at one of a plurality of address encoders, the memory request including a register index input and a processor mode input;

encoding the register index input and processor mode input at the one of the plurality of address encoders to obtain an encoded address;

accessing at least one of the memory locations of the unbanked memory unit in accordance with the encoded address, wherein the encoded address corresponds to at least one register and processor mode; and

writing data into or reading data from the accessed memory location.

79. (Original) The method of claim 78, wherein writing data into or reading data from the accessed memory location includes writing data into or reading data from the accessed memory location for multiple instructions,

80-85. (Cancelled)

IX. EVIDENCE APPENDIX

A copy of the Office Action mailed August 15, 2008 is attached.

X. RELATED PROCEEDINGS APPENDIX

None.